In the Claims:

Please amend claims 31 and 32. The claims are as follows:

1. (Canceled)

2. (Previously Presented) The computer system of claim 31, wherein said simulated external memory mapped test device and said simulated switch are distributed among a plurality of simulated external memory mapped test device modules, each module of said plurality of simulated external memory mapped test device modules containing a portion of said simulated switch and connected to a respective second external I/O driver model of said second external I/O driver models.

3. (Previously Presented) The computer system of claim 31, wherein said simulated external memory mapped test device further includes a simulated address register.

4. (Canceled)

5. (Previously Presented) The computer system of claim 2, wherein each said simulated external memory mapped test device module further includes a simulated address register.

6. (Canceled)

7. (Previously Presented) The computer system of claim 31, wherein said simulated external memory mapped test device and said simulated switch are distributed among a plurality of

simulated external memory mapped test device modules, each module of said plurality of simulated external memory mapped test device modules containing a portion of said simulated switch and connected to a respective second external I/O driver model of said one or more second external I/O driver models; and

executing said instructions causes the computer to perform the further following steps:

loading code representing an additional simulated external memory mapped test device module into said memory unit;

said loading of said test case connecting one or more additional second external I/O driver models to said additional simulated external memory mapped test device by additional simulated I/O buses; and

said loading of said test case connecting each additional second external I/O driver model to a respective additional simulated I/O core by said simulated system bus, each additional simulated I/O core comprising said model of integrated circuit design.

8-15 (Canceled)

16. (Previously Presented) The program product of claim 32, wherein said simulated external memory mapped test device and said simulated switch are distributed among a plurality of simulated external memory mapped test device modules, each module of said plurality of simulated external memory modules containing a portion of said simulated switch and connected to one of said simulated I/O driver models.

17. (Previously Presented) The program product of claim 32 wherein said simulated external memory mapped test device includes a simulated address register; and

executing said instructions, further causes said computer to connect said simulated switch to one second external I/O driver model of said one or more second external I/O driver models using address information programmed into said simulated address register.

18. (Canceled)

19. (Previously Presented) The program product of claim 16, wherein each simulated external memory mapped test device includes a corresponding simulated address register; and

executing said instructions, further causes said computer to connect each portion of said simulated switch to one second external I/O driver model of said one or more I/O driver models using address information programmed into its corresponding simulated address register.

20. (Canceled)

21. (Previously Presented) The computer system of claim 31, wherein said one or more simulated I/O cores are each independently selected from the group consisting of a simulated 1394 I/O core, a simulated universal asynchronous receiver transmitter core, a simulated serial core, a simulated general purpose I/O core, and a direct memory access core.

22 -30 (Canceled)

31. (Currently Amended) A computer system comprising a processor and a computer-readable memory unit coupled to communicate with said processor, said memory unit containing instructions that when executed by the processor causes the computer to perform the following steps:

loading code representing said integrated circuit design into said memory unit, said integrated circuit design including simulated I/O cores, a simulated memory controller, a simulated I/O controller, a simulated bus system and a simulated processor, said simulated I/O cores and said simulated I/O controller connected to said simulated processor by said simulated system bus;

loading into said memory unit, code representing (i) an external memory model connected to a simulated external memory mapped test device and to said simulated memory controller, (ii) one or more first external I/O driver models connected between said simulated I/O cores and said simulated external memory mapped test device and (iii) one or more second external I/O driver models connected between a simulated switch of said simulated external memory mapped test device and said I/O controller, said simulated switch programmably connectable to said one or more second external I/O driver models in response to computer-executable instructions in a test case, all said connections of (i), (ii) and (iii) by corresponding simulated I/O buses;

loading said test case , said test case comprising said list of computer-executable instructions for said simulated processor into said external memory model, said instructions describing selection of one or more simulated I/O cores and corresponding second external I/O models, allocation of pins of said I/O controller to selected simulated I/O cores and switch

positions of said simulated switch to connect said corresponding second external I/O models to said I/O controller;

executing said test case and allocating and connecting I/O pins of said simulated I/O controller to one or more of said simulated I/O cores, and connecting said simulated external memory mapped test device to said simulated I/O controller through said corresponding second external I/O models executing test stimuli of said test case on said simulated processor in order to generate data representing a response of said computer simulation model of said integrated circuit design to said test case; and

outputting said data representing (iv) a response of said computer simulation model of said integrated circuit design to said test case to another computer readable media or another computer, (~~ii~~ v) display said data representing a response of said computer simulation model of said integrated circuit design on a computer screen, or both (iv) and (~~ii~~ v).

32. (Currently Amended) A computer program product embodied on a computer readable medium comprising code that, when executed, causes a computer to perform the following:

load a model of said integrated circuit design into a memory of said computer, said integrated circuit design including simulated I/O cores including a simulated general purpose core, a simulated external memory controller, a simulated I/O controller, a simulated bus system and a simulated processor, said simulated I/O cores and said simulated I/O controller connected to said simulated processor by said simulated system bus;

load into said memory unit, code representing (i) an external memory model connected to a simulated external memory mapped test device and to said simulated memory controller, (ii) one or more first external I/O driver models connected between said simulated I/O cores and said

simulated external memory mapped test device and (iii) one or more second external I/O driver models connected between a simulated switch of said simulated external memory mapped test device and said I/O controller, said simulated switch programmably connectable to said one or more second external I/O driver models in response to computer-executable instructions in a test case, all said connections of (i), (ii) and (iii) by corresponding simulated I/O buses;

load said test case, said test case comprising said list of computer-executable instructions for said simulated processor into said external memory model, said instructions describing selection of one or more simulated I/O cores and corresponding second external I/O models, allocation of pins of said I/O controller to selected simulated I/O cores and switch positions of said simulated switch to connect said corresponding second external I/O models to said I/O controller;

executing said test case and allocating and connecting I/O pins of said simulated I/O controller to one or more of said simulated I/O cores, and connecting said simulated external memory mapped test device to said simulated I/O controller through said corresponding second external I/O models;

execute test stimuli of said test case on said simulated processor;

generate data representing a response of said computer simulation model of said integrated circuit design to said test case; and

(iv) output said data representing a response of said computer simulation model of said integrated circuit design to said test case to another computer readable media or another computer, (~~ii~~ v) display said data representing a response of said computer simulation model of said integrated circuit design on a computer screen, or both (iv) and (~~ii~~ v).

33-36 (Canceled)